FeRAM Technology

FeRAM is widely considered as the ideal non-volatile memory with highly desired performance features such as high write speeds, low power operation and high endurance (read-write cycles) and is comparable in cell size to other existing and emerging non-volatile memory technologies. FeRAMs also have an added significant advantage, which is high radiation hardness. FeRAMs are inherently radiation-hard making it very suitable for space applications.

Conventionally, FeRAM architecture is very similar to that of Dynamic Random Access Memory (DRAM) architectures with true random access. The memory element in FeRAMs is a ferroelectric capacitor (the ferroelectric material sandwiched between two metal electrodes) very much like the memory element in DRAMs, where a dielectric material is sandwiched between two metal electrodes. The ferroelectric material is a dielectric material as well. However, ferroelectrics have an added feature, which is the capability to retain the logic state that it is being written into for a long time (typically greater than 10 years). DRAMs on the other hand, requires refresh in the order of milliseconds (ms) to retain the state.

The ferroelectric material typically has a perovskite (ABO_3) lattice structure like the one shown in Figure 1. The atoms in the corner of the unit cell represent the larger cations ('A'), the atom in the center represent the smaller cation ('B'),

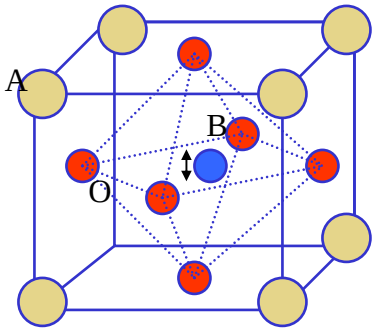
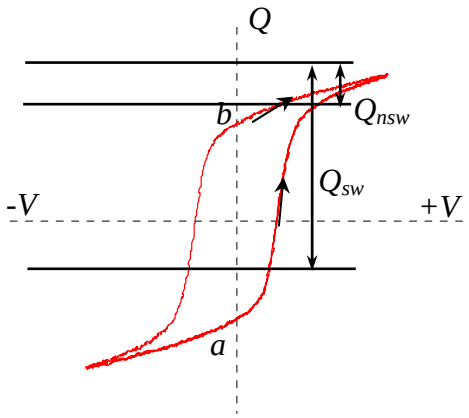


Figure 1. A perovskite unit cell

typically with a larger charge and the anions (O_3) on the six face centers. The stable state of the ferroelectric capacitor is achieved by displacement (in the order of sub-tenth of an angstrom) of the 'B' cation with respect to the anions. This in effect forms a dipole. This displacement can be achieved with the help of an electric field applied between top and bottom metallic plates in between which the ferroelectric material is sandwiched. The collective charge displacement amongst many such unit cells can then be sensed as a current flowing between the electrodes of the ferroelectric capacitor.

The charge displacement is often expressed in the form of a hysteresis or a *Q*-*V* curve (Figure 2). The capacitor can be placed in a desired state ('*a*' or '*b*') during a *write* operation by applying appropriate voltage and polarity. During a *read* operation, assuming the current state of the ferroelectric capacitor is in a remnant state '*a*' (negatively polarized corresponding to logic state '*0*'), applying a positive field to read



Positive field to state 'a'
States switched
Charge displacement is Q_{sw}

Positive field to state 'b'
States not switched
Charge displacement is Q_{nsw}

Memory Window - $Q_{sw} \sim Q_{nsw}$

Figure 2. Hysteresis Curve (Q-V) of a ferroelectric material

the state of the capacitor displaces the center ion to the positive state. This results in a specific current flow, which can be referenced against a fixed state with the help of a sense amplifier to identify the state. When the positive field is removed, there is a slight relaxation to remnant state '*b*', but the center ion remains in the positive state. If the current state of the capacitor is in remnant state '*b*' (positively polarized corresponding to logic state '*1*'), applying a positive

field to the capacitor does not displace the ion and hence the resulting current flow is relatively smaller. The difference in the magnitude of these displacements, i.e., memory window (reading from remnant states '*a*' and '*b*'), helps in identifying the state of the capacitor. In 1T/1C type architecture, typically the reference state is usually in the middle of the memory window and in 2T/2C type architecture, one cell is referenced over another cell that is always in a complementary state. Obviously, the memory window is wider for 2T/2C type architecture.

The parametric testing for ferroelectric capacitors include testing for polarization values (the memory window), the minimum electric field required to switch the ferroelectric from one state to the other and leakage current density thought the ferroelectric. In addition to the parametric testing, the characterization for reliability of FeRAMs includes fatigue, retention and imprint. Fatigue is defined as decrease in polarization with repeated number of switching cycles, retention is defined as the time period that the programmed state is retained in the ferroelectric at a specific temperature and imprint is defined as the preference of the memory towards one state over the other.